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COMPLETE SPECIFICATION.

Improvements in or relating to Circuit Arrangements for the Transfer of Energy from one Store to another Store.

We, SIEMENS & HALSKE AKTIENGESELLSCHAFT, a German Company of Berlin and Munich, Germany, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The invention relates to circuit arrangements for the transfer of energy from one store to another.

Such circuit arrangements may in particular be employed in exchange systems operating on the time-division multiplex principle as used in telephone work. A time-division multiplex exchange system is characterised by the fact that the information to be exchanged is modulated on staggered pulse trains, thus enabling multiple exploitation of trunk lines and control equipment. In the event of demands for connections being made, the subscribers concerned are connected together in pairs through at least one multiplex rail. To effect this, switches belonging to the subscribers concerned in a connection are closed synchronously under control of pulses of the staggered pulse trains.

During the pulse intervals the switches are open. These switches can be located for instance in line sections leading to subscriber stations. Due to the special mode of operation of the circuit concerned, the open times of the switches are in each case substantially longer than the times for which they are closed. Energy can, of course, only be transmitted by these switches when they are closed so that the process of energy transfer is a pulse process. Due to the long open times, however, the energy transfer process suffers severe attenuation if special measures are not taken to combat this.

In order to prevent any such adverse influencing of the energy transfer process, the method is already known whereby reactive networks are allotted to the said switches (see Patent Specification No. 822,297). The line sections which are to be connected with one another *via* switches, are here terminated in capacitors which serve as energy stores. The charge in each case built up in such capacitor, is transferred *via* at least one series coil to a capacitor terminating another line section. This procedure has long been known (see the book "Pulse Generator", by G. N. Glasoe, New York and London, 1948, Pages 307 and 308, in particular Figures 8.17 and 8.18). In this book, an explanation is given of how a series coil inserted in the electrical circuit enables complete discharge to take place by virtue of a resonance effect.

The energy transfer processes under consideration can also be effected *via* what are known as intermediate stores. An intermediate store of this type is alternately connected with the capacitors terminating the line sections, *via* a series coil. In this way, there is in each case an exchange of energy between the capacitor belonging to a given line section and the intermediate store. If the intermediate store it itself a capacitor, then this exchange of energy is in the form of an exchange of charge, each of the capacitors simultaneously discharging and at the same time charging up the other. These two processes are super-

imposed on one another. In order that there should be no interference, the circuit elements associated with this process must have highly linear properties, *i.e.* their electrical properties such as capacitance, inductance and so on, must be independent of the particular current or voltage obtaining at any time.

The invention now demonstrates a way in which to overcome the need for the condition that the intermediate stores used are highly linear in operation. In this case, there is no need for an intermediate store simultaneously to receive energy from the capacitor connected to it by a coil and to itself transfer energy to this capacitor. With the removal of these conditions, the requirements governing the appropriate properties of the intermediate store are less stringent so that stores of a type other than that usually employed may be used. As will be shown later, it is then possible for instance to employ intermediate stores which have amplifying properties. This prevents the development of undesired parasitic signal frequencies such as would otherwise come into evidence when superimposing different oscillations on one another in circuit elements which are not strictly linear. For these various reasons, the invention constitutes a significant addition to the state of technology.

It should be pointed out that the line sections to be linked *via* the circuit proposed in accordance with the invention, may belong to devices other than a telephone exchange system. For instance, they can form part of a transmission system such as a multi-channel programme transmission system for radio purposes (see German Patent 1,084,329). There, signals belonging to two separate stereo channels have to be correctly transmitted to the appropriate line sections.

The invention consists in a circuit arrangement for the transfer of energy from a first store to a second store, including first and second store switching means capable of connecting the first store to a first multiplex rail and the second store to a second multiplex rail and including two intermediate stores and intermediate store switching means capable of connecting either one intermediate store to the first multiplex rail and the other intermediate store to the second multiplex rail or said one intermediate store to the second multiplex rail and said other intermediate store to the first multiplex rail, the arrangement being such that in operation the first store is connected to said one intermediate store through the first multiplex rail and the second store is connected to said other intermediate store through the second multiplex rail and any energy stored in the first and second stores is transferred to the intermediate stores, whereafter said one intermediate store is connected to the second store through the second multiplex rail and said other intermediate store is connected to the first store through the first multiplex rail to complete the energy interchange between the first and second stores.

The presence of two multiplex rails means that in the event of a fault which renders one multiplex rail inoperative due say to shorting to earth or to other short-circuiting, emergency operation through one multiplex rail only is possible by slightly modifying the pattern of operation of the switch means.

There follows a description by way of example of a method of performing the invention with reference to the accompanying drawings in which:

Figure 1 is an exemplary embodiment of a time-division multiplex telephone exchange system embodying the invention in which line stores are constituted by capacitors;

Figures 2, 3, 4 and 14 illustrate various types of intermediate stores;

Figure 5 is an exemplary embodiment of a time-division multiplex telephone exchange system embodying the invention in which special measures have been adopted to prevent the undesired backflow of transferred energy;

Figures 6, 7 and 8 are examples of timing diagrams relating to the operation of various switches and to the energy transfer processes in each case involved;

Figures 9 and 10 illustrate examples of arrangements of capacitors and coils for use as parametric amplifiers;

Figures 11 and 13 are timing diagrams illustrating how switches are operated and how the associated energy transfer processes take place, when only one multiplex rail is in action; and

Figure 12 illustrates a circuit corresponding substantially to Figure 5, but in which only one multiplex rail is operative.

In Figure 1, several line stores may be connected to the multiplex rails *Man* and *Mab;* these stores terminate line sections such as the two line sections *Ta* and *Tb* illustrated. The line stores *Ca* and *Cb* belong to these latter two line sections. The line store *Ca* is in this case connectable *via* the switch *anta* to the multiplex rail *Man* and *via* the switch *abta* to the multiplex rail *Mab*. The line store *Cb*, similarly, is connectable *via* the switch *antb* to the multiplex rail *Man* and *via* the switch *abtb* to the multiplex rail *Mab*. The multiplex rail *Mab* serves as the outgoing multiplex rail through which outgoing traffic is conducted. This means that line

sections from which a connection is to be developed in the outgoing direction should be connected *via* their appropriate switches to this multiplex rail. The multiplex rail *Man* serves as the incoming multiplex rail. This means that line sections to which a connection is to be developed in the incoming direction, should be connected to this rail *via* their appropriate switches. Thus, by the connection in each case of the appropriate line section or line store to one or other of the multiplex rails, a distinction is drawn between outgoing and incoming directions of development of a connection.

The switches used to establish such connection may be operated with the aid of a train of control pulses, in known fashion (*e.g.* see French Patent No. 1,072,144). Since one of the two line stores concerned is connected to one multiplex rail and the other line store is connected simultaneously to the other, the same control pulse can be employed for operating both the switches involved.

The line stores serve on the one hand to collect the energy arriving through the appropriate line section during the pauses occurring in the course of the pulse-type transfer processes, and on the other hand to rapidly store the energy transferred to them during such a transfer process, later passing it on through the appropriate line section during a subsequent pause in the transfer process. Capacitors are particularly suitable for the line stores. These capacitors exchange their charges in the course of energy transfer. On completion of the transfer process, both the capacitors involved and operating as line stores, will have exchanged their charges with one another. Also included between the line stores and the appropriate line sections, are low-pass filters embodying the chokes *Da* and *Db* and the capacitors *a*C and *b*C. The cut-off frequency of these filters is less than half the control pulse train frequency for the switches allotted to the line stores, with the result that the pulse train frequency is suppressed by these filters.

In the energy transmission path from one line store to another, two intermediate stores S1 and S2 are included. They are connectable to the multiplex rails by means of the switches 1*k*1, 2*k*1, 1*k*2 and 2*k*2. By suitably operating the two switches concerned, these two intermediate stores can be alternately connected to the two multiplex rails during the time for which the appropriate line stores are likewise so connected. The circumstance that two intermediate stores and two multiplex rails are provided, makes possible a procedure whereby energy is transmitted along separate transmission paths simultaneously from one line store to one intermediate store and from the other line store to the other intermediate store. Then, likewise, the energy received in the intermediate stores can be transferred from the one intermediate store to the other line store and from the other intermediate store to the line store first considered. The two line stores concerned will then have exchanged their energy contents with one another. All these energy transfer processes can be completed quite separately from one another. In each of the circuits formed for this purpose only one energy transfer process takes place. If the switches allotted to the line stores and to the intermediate stores are operated in proper sequence, then energy transfer takes place only in stores which have previously been emptied. Any two line sections can be involved in these energy transfer processes, since all such sections are similarly connected to the two multiplex rails *Man* and *Mab*. The presence of more than two lines is indicated by the multi-connection sign. In each case too, intermediate storage of the energy to be transferred takes place. The intermediate storage of transferred energy can be associated with amplification. This will be explained more particularly later making reference to examples.

Intermediate stores of various types can be used in a circuit in accordance with the invention. For instance, the intermediate stores may take the form of inductive coils. Then, between the points X and Y of the circuit of Figure 1, the coils L1 and L2 of Figure 2 are inserted.

Where the line stores are in the form of capacitors, energy transfer to the store concerned in each case takes the form of a quarter cycle oscillation in the oscillatory circuit which is established when the switch is operated. The way in which the switches involved are operated, is illustrated in the timing diagrams of Figure 6. In these timing diagrams the time axis is horizontal, with increasing time plotted towards the right. In the diagram T, an illustration is given of when the switches *abta* and *antb* allotted to the line sections T*a* and T*b*, are operated. Here, the line section T*a* is handling outgoing traffic and the line section T*b* incoming traffic. If the line section T*a* were handling incoming traffic and the line section T*b* outgoing traffic, then the switches *anta* and *abtb* would have to be operated. Whatever the case, the two switches concerned must be operated simultaneously. During the time of operation of the switches *abta* and *antb*, the coils L1 and L2 are alternately connected to the two multiplex rails *Man* and *Mab*, firstly *via* the switches 1*k*1 *and* 2*k*2 and subsequently *via* the switches 2*k*1 and

1k2. The way in which these switches operate is depicted in the diagrams K1 and K2. The diagram K1 shows how the coil L1 is first of all connected to the outgoing multiplex rail *Mab via* the switch 1k1. Immediately on completion of the operation of this switch, the switch 2k1 closes, connecting the coil L1 to the incoming multiplex rail *Man*. Similarly, in the diagram K2, it is shown how the coil L2, during the time of operation of the switches *abta* and *antb*, is connected *via* the switch 2k2 to the incoming multiplex rail *Man* and immediately thereafter to the outgoing multiplex rail *Mab*. Thus, at any given time only one of these two coils is connected to one and the same multiplex rails.

The times of operation of the switches 1*k*1, 2*k*1, 1*k*2 and 2*k*2 allotted to the coils serving as intermediate stores, are in this case no more than half as long as the times of operation of the switches allotted to the line sections. Thus, they could be even shorter than indicated in the diagrams K1 and K2, as long as the periodic times of the oscillatory circuits constituting the particular transmission paths, these oscillatory circuits being constituted by the capacitors serving as line stores and by the coils serving as intermediate stores, are correspondingly higher. The time of operation of the switches 1*k*1, 2*k*1, 1*k*2 and 2*k*2 should in this case be so arranged that energy transfer in the form of a precise quarter cycle oscillation can take place. The times of operation of the switches allotted to the line sections, as illustrated in the diagram T (Figure 6), can however vary without in any way disturbing the process, and this variation is indicated by time intervals Δt. Thus, there are no very stringent requirements on the accuracy of these operating times. On the other hand, the operating times of the switches 1*k*1, 2*k*1, 1*k*2 and 2*k*2 should be held to relatively fine limits. Since these switches are centrally located and there are only four switches irrespective of the number of lines, this is not difficult to achieve for a modest outlay. For the same reason, particularly short operating times are possible.

Making reference to the diagrams *uCa*, *uCb*, *i*L1, and *i*L2, also portrayed in Figure 6, the behaviour of the voltages across the capacitors *Ca* and *Cb* serving as line stores as well as the behaviour of the currents in the coils L1 and L2 serving as intermediate stores, can be studied. First of all the coil L1 will be considered. In the first place it is connected *via* the switch 1*k*1, *via* the outgoing multiplex rail *Mab* and *via* the switch *abta*, to the capacitor *Ca*. This capacitor discharges (see diagram *uCa*), so that the current through the coil L1 rises to a maximum in the course of a quarter cycle oscillation, as the diagram *i*L1 shows. At this instant, the energy hitherto stored in the capacitor *Ca* has been transferred to the coil L1 where it is now available in magnetic form. At the same instant, the switch 1*k*1 opens and the switch 2*k*1 closes. The current then flows on without interruption, and the previous energy transfer process from the capacitor *Ca* to the coil L1 is followed directly by energy transfer from this coil to the capacitor *Cb*, the latter in this case being the other line store concerned; for this second energy transfer process capacitor *Cb* is connected *via* the switch *antb*, *via* the incoming multiplex rail *Man* and *via* the switch 2*k*1, with the coil L1. The current through the coil L1 falls and the voltage across the capacitor *Cb* rises, as the diagrams *i*L1 and *uCb* show. Prior to this, the capacitor *Cb* has been discharged into the coil L2 as described below; by operating a switch 2*k*2, the coil L2 is connected to the capacitor *Cb via* the switch *antb*, and *via* the incoming multiplex rail *Man*, thus bringing about the aforesaid discharge. This causes a similar rise in the current through the coil L2, during a quarter cycle oscillation, reaching a maximum as indicated in the diagram *i*L2. Immediately on completion of the time of operation of the switch 2*k*2, the switch 1*k*2 is operated, connecting the coil L2 *via* the outgoing multiplex rail *Mab* and *via* the previously closed switch *abta*, to the capacitor *Ca*. The current in the coil L2 falls off in the process, whilst the capacitor *Ca* is charged up. This is indicated by the diagrams *i*L2 and *uCa*. On completion of all these switching operations, the two capacitor *Ca* and *Cb* have exchanged their charges with one another and consequently the voltages across them are exchanged (assuming equal capacitances). The coils L1 and L2 at this point carry no current. The initial conditions are now reversed and the capacitor *Ca* formally having the lower voltage now carries the higher voltage and the capacitor *Cb* formally carrying the higher voltage now carries the lower one.

Further special measures may be adopted in order to ensure that in no circumstances can any interruption take place in the flow of current through either of the coils L1 and L2 during the successive energy transfer processes concerned. To this end, a coil serving as intermediate store can have an auxiliary capacitor connected in parallel with it, this momentarily carrying a current. Auxiliary capacitors of this type are indicated in Figure 2 connected up by broken-lines and designated *c*1 and *c*2. It may be advisable to periodically short-circuit these auxiliary capacitors at suit-

able instants, in order to prevent the accumulation of any charge. The coils L1 and L2 can also be employed for parametric amplification purposes. The manner in which parametric amplification can be effected will be discussed later on.

First of all, discussion will be made of a number of further measures which, where capacitors are used as line stores and where the intermediate stores employed are other than the coils previously referred to, improve the pulse-type energy transfer process. First of these measures is the provision of inductive coils which are in each case included in the energy transmission paths when the switches are operated and, due to their inductance, effect energy transfer to the store concerned in the form of a part oscillation. These coils may be centrally located. Here again, there are several possibilities. For instance, the coils may be connected directly in series with the intermediate stores, as illustrated in the circuit of Figure 3 where the coils 1L and 2L are in series with the capacitors C1 and C2 serving as intermediate stores. Alternatively, however, at least a part of each centrally located coil can be arranged in a multiplex rail. For instance, coils *Lan* and *Lab* can be thus arranged in the multiplex rails *Man* and *Mab* of the circuit illustrated in Figure 5. In place of centrally located coils, coils in a decentralised arrangement may be used. In this case, they are arranged between the line stores allotted to the line sections, and the multiplex rails. Thus, in the circuit of Figure 5, the coils *La* and *Lb* are inserted between the line stores *Ca* and *Cb* and the multiplex rails *Man* and *Mab*. If these coils are present, then any energy transfer process must take place *via* at least one such coil so that due to the inductive effect the advantage of lossless limiting of the associated current is obtained. The effective inductance can in each case be distributed amongst a centrally located coil and a de-centralised coil. In the case under consideration, all the coils illustrated in Figure 5 are active in the circuit shown here.

Conveniently, the central coil and/or the de-centralised coils will be formed as parametric amplifiers. In this way, energy transfer can be associated with amplification, whereby circuit and other losses can be compensated for. An inductive coil can, where the inductance is controlled, effect amplification of the energy transmitted through it (*e.g.* see Fernmelde-praxis, Volume 37, No. 6, 15.3.1960, Pages 201 to 228, in particular 227; Bulletin des schweiz-electrotechn. 1960, Pages 1046 to 1053, Proceedings of the I.R.E., July 1956, Pages 904 to 913, and May 1958, Pages 850 to 886). For this purpose, the coil may be subdivided into part coils having several windings. If the coil concerned is a centrally located one which does not at the same time serve as an intermediate store, then there is particular advantage in the fact that the gain factor of this coil, when acting as a parametric amplifier, follows a square law where the energy transfer between the two separate line stores is concerned. As already explained, energy transfer in each case takes place in two stages *via* an intermediate store. Thus, it passes on each occasion through the central coil considered and is therefore amplified each time. The de-centralised coils can also operate as parametric amplifiers. Since the energy transfer from a line store to another line store in this case takes place *via* the two coils allotted to the two line stores concerned, it is the product of the two gain factors which is of importance. It should be noted that the operating time of the switches may need to be adapted to change in the resonant frequency of the oscillatory circuits concerned resulting from the parametric amplification effect.

As already indicated, intermediate stores of various types can be employed in a circuit such as that proposed in accordance with the invention. For instance, the intermediate stores can also be formed as capacitors. Then, the capacitors C1 and C2 should be inserted between the points X and Y in the circuit of Figure 1, these capacitors being illustrated in Figure 3. In series with these capacitors, are the coils 1L and 2L, whose inductance plays a part in the energy transfer process. Energy transfer from and to the capacitors acting as line stores then takes place in the form of a half cycle oscillation. Capacitors operating as intermediate stores can also be designed for parametric amplification. To achieve parametric amplification, the capacitance of the capacitor concerned must be reduced prior to discharge. The energy required to bring this about serves to increase the energy content of the capacitor. Capacitors suitable for this purpose are already known (*e.g.* see Fernmelde-praxis, Volume 37, No. 6, 15.3.1960, Page 227). A capacitor of this type can also be subdivided into several part capacitors. With the aid of intermediate stores which also act as parametric amplifiers, losses in the circuit as well as other transmission losses can be compensated for.

Frequently, it is convenient to short-circuit the capacitors serving as intermediate stores using appropriate switches, prior to receiving a charge from a line store. Short-circuiting switches of this type are provided in the circuit illustrated in Figure

5 and are designated by $k1$ and $k2$. With the aid of these switches, any residual energy which, due to some fault, has remained from the previous energy transfer process, is prevented from interfering with or distorting a succeeding energy transfer process. For similar reasons, it is recommended that with this circuit example and the others which will be discussed later on, periodic earthing of the multiplex rails be effected at suitable instants.

The intermediate stores may alternatively take the form of ferromagnetic cores. In this case, they should be made of a material exhibiting remanence properties and having an approximately linear magnetic working characteristic within the range which is to be employed for the in-storage of energy.

When storing energy into such a core store, the store passes from a fixed predetermined initial magnetic state to a new one, and is maintained thus until out-storage takes place. This second state of magnetisation in each case corresponds to the energy being transferred. When out-storage takes place, energy transfer is effected from the core store to a line store. This energy transfer is brought about with the aid of a read pulse which re-sets the core store concerned to its initial magnetic state. Where core stores of this type are used, between the points X and Y in the circuit of Figure 1, the core stores K1 and K2 illustrated in Figure 4 should be inserted. The read pulses are in this case fed to the windings connected to the pairs of terminals $p1$ and $p2$. Here again, it may be convenient to supply special re-set pulses to the core stores (intermediate stores) before in-storage of energy takes place. These re-set impulses too should be supplied *via* the pairs of terminals $p1$ and $p2$. With their help, the cores are in each case re-set precisely to their fixed initial magnetic state.

The intermediate stores can also take the form of superconductive coils in which, in the course of in-storage of energy, a current is induced *via* coupling coils. Due to the superconductivity phenomenon, this current is then maintained until out-storage takes place. Figure 14 illustrates an example of the use of intermediate stores of this type. They should be connected *via* the terminals A and B to the point X and Y in the circuit of Figure 1, in place of the intermediate stores S1 and S2. The superconductive coils are designated $Sa2$ and $Sb2$. They may have one or more windings. The coupling coils are designated by $Sa1$ and $Sb1$. The superconductive coils $Sa2$ and $Sb2$ are each surrounded by a read winding. For purposes of energy transfer from a superconductive coil to a line store, the appropriate read winding is supplied with a read pulse from the pulse generator Pa/Pb, which pulse during the period of its existence produces a magnetic field which nullifies the superconductivity of the inner coil (see K. Steinbuch: Taschenbuch der Nachrichtenverarbeitung, 1962, Page 645 in particular Figure 4.10/2). This results in the disappearance of the current flowing through the inner coil and the collapse of its magnetic field produces in the associated coupling coil an output pulse which is fed to the appropriate line store. Diagram k of Figure 13 gives an example of the timing of such read pulses, they are indicated by pa and pb. This Figure will be discussed in greater detail later. The magnetic field produced by the read pulse has no effect on the coupling coil since the windings of the read coil are perpendicular to it. Thus, we are concerned here with a novel application of superconductivity in coils which in themselves are of functional significance.

If ferromagnetic cores or superconductive coils are employed as intermediate stores, then any inductive properties they possess may be exploited to contribute to the complete discharging of capacitors serving as line stores, within a short space of time. In this way, coils having lower than usual inductance can be inserted in the transmission paths or such coils can be omitted altogether.

It is pointed out also that where the intermediate stores are in the form of capacitors or cores or other components, the times of operation of the switches allotted to them should be no more than half as long as the times of operation of the switches allotted to the line sections.

In the following, the mode of operation of the circuit illustrated in Figure 1 will be described, if the capacitors C1 and C2 of Figure 3 are employed as intermediate stores, these capacitors being in series with the coils 1L and 2L. The energy transfer processes to the store concerned here take place in the form of a half cycle oscillation in the oscillatory circuits brought into being at any instant by operation of the switches. These energy transfer processes and the sequence of operation of the switches concerned are portrayed individually in the timing diagrams of Figure 7. In the diagrams marked T, K1 and K2, the operation of the appropriate switches is illustrated. These three diagrams are largely the same as the corresponding ones illustrated in Figure 6. Accordingly, the operating conditions for the switches are also largely the same in both cases. The sole difference lies in the fact that in the case now under consideration the switches $1k1$ and $2k1$, or $2k2$ and $1k1$, are no longer

operated immediately after one another, instead there may be a pause between the operative times since the energy stored in a capacitor (intermediate store) in the form of a charge cannot immediately be passed on. Allowance for such a pause is made in the diagrams K1 and K2.

During the times of operation of the switches 1*k*1, 2*k*1, 1*k*2 and 2*k*2, as already mentioned, energy processes in the form of a half cycle oscillation take place. The associated behaviour of the voltages across the capacitors *Ca* and *Cb* as well as the behaviour of the charge and discharge currents associated with the capacitors C1 and C2 serving as intermediate stores, is portrayed in the diagrams *u*C*a*, *u*C*b*, *i*C1 and *i*C2 of Figure 7. The diagram *u*C*a* illustrates the behaviour of the voltage across the capacitor C*a*. It will be seen that the voltage initially appearing across this capacitor disappears when the switch 1*k*1 is operated. Simultaneously, as the diagram *i*C1 shows, the capacitor C1 is charged up by a current of half-wave form. During the simultaneous operation of switch 2*k*2, the voltage across the capacitor C*b* disappears, see diagram *u*C*b*. Simultaneously, as the diagram *i*C2 shows, the capacitor C2 is charged up by a current of half-wave form. This is followed by the simultaneous operation of the switches 2*k*1 and 1*k*2. The operation of the switch 2*k*1 results in the discharge of the capacitor C1 (see diagram *i*C1) and in the charging up of the capacitor C*b* (diagram *u*C*b*). Operation of the switch 1*k*2 results in similar processes for the capacitors C2 and C*a*, see the diagrams *i*C2 and *u*C*a*. The voltages across the capacitors C*a* and C*b* at the commencement of the energy transfer processes were different. The capacitor C*a* was at the lower voltage and the capacitor C*b* was at the higher one. On completion of the energy transfer processes just described, the capacitor C*a* has the higher voltage across it and the capacitor C*b* the lower one. The capacitors have exchanged their charges.

As already described in considerable detail, ferromagnetic cores can also be employed as intermediate stores. In this case, read pulses are required in order to outstore the energy from the cores. Although the behaviour of the currents and voltages obtaining during energy transfer is in this case somewhat different from that obtaining when capacitors are used, the principle is very similar.

As already mentioned, where capacitors are used for the line stores and where energy transfer takes place in the form of half cycle or quarter cycle oscillations, the times of operation of the switches allotted to the intermediate stores must in particular be adapted to the period of duration of the said partial oscillations. If the operating time is too short, then the energy transfer is incomplete as part of the energy remains in the store which was supposed to be discharged. If the operating time is too long, however, then at least part of the transferred energy flows back to the store from which it has just come. Also, the switch concerned must open at the right instant in order to prevent further energy transfers through which part at least of the energy transferred just previously would arrive at wrong destinations, in particular at other line sections whose switches happened to be operated. This might lead to cross-talk between different connection paths. However, the aforementioned conditions governing the operation of the switches concerned may be relaxed somewhat if specific additional measures are adopted. These are not obvious measures. They are considered in the context of a circuit in which capacitors are used as line stores. If, in this circuit, energy transfer processes are carried out exclusively in the form of pulses of greater or lesser amplitude and of one polarity only, then for our purpose rectifiers may be inserted in the transmission paths, whose polarity is so arranged that they only pass the current pulses constituting the intended energy transfer in the forward direction. By adapting this measure, in many cases the times of operation of the switches can be allowed to vary within relatively wide limits without any risk that a backflow of energy will take place after the desired energy transfer process has been completed. This is prevented by the rectifiers which have the effect of blocking any such tendency. If capacitors are employed as intermediate stores, and coils are also inserted in the transmission paths, the second half cycle oscillation, following the first such oscillation during which the capacitor concerned is charged up, is suppressed. Consequently, no undesired direct discharge of this capacitor is possible. Then, inaccurate opening of the switch concerned is less serious than usual since in this case too, any discharge of the capacitor just charged up is prevented. Thus, the insertion of rectifiers combats cross-talk effects. It can also be advantageous to include rectifiers when other types of intermediate stores are used, if there is a risk of the undesired reverse flow of energy which has just been transferred. If inductive coils are employed as intermediate stores, then by inserting the rectifiers, after out-storage of the energy content of the coil concerned to a capacitor serving as line store during a quarter cycle oscillation, undesired reverse flow of the energy stored in the capacitor is prevented.

The presence of rectifiers in the trans-

mission paths in each case developed, as proposed in the foregoing, can be effected in various ways. For instance, the provision can be made that each intermediate store is connectable to each multiplex rail *via* appropriate switches, these switches each being in series with a differently polarised rectifier so that the rectifier polarised rectifier so that the rectifier appropriate to the desired direction of energy transfer can be included in the transmission path. This measure is adopted in the circuit of Figure 5. As can be seen, there is a rectifier in series with each of the switches 1*k*1, 2*k*1, 1*k*2 and 2*k*2. These rectifiers are designated by 1G1, 2G1, 1G2 and 2G2. If, for placing the intermediate stores in circuit, the switches used are of a type which basically only permit energy transfer in the desired direction and therefore already embody the rectifier function, then separate rectifiers are of course unnecessary.

Thus far, it has been assumed that pulses of exclusively one polarity are involved in the energy transfer processes. If this is basically not the case, then the same result can nevertheless be achieved by using special measures, even where alternating voltages and currents of different frequency are to be transmitted through the particular connection established. Consider a circuit in which low-pass filters are connected before the line stores. These low-pass filters are connected to the appropriate line sections *via* transformers. The primary windings of these transformers are supplied with the *a.c.* voltages it is desired to transmit. To the secondary windings of these transformers, a bias voltage is applied having an amplitude at least equivalent to the highest *a.c.* amplitude to be transmitted and having the same polarity as the charges which appear in the capacitors serving as line stores.

This measure too is adopted in the circuit of Figure 5. There, low-pass filters are connected before each of the capacitors *Ca* and *Cb* serving as line stores, these comprising the chokes D*a* and D*b* and the capacitors *a*C and *b*C. The transformer W*a* is associated with the line section T*a* to which the line store C*a* belongs. To its secondary winding II a positive bias voltage +U is applied. The *a.c.* voltages and currents to be transmitted are supplied to the primary winding I of this transformer. Similarly, the transformer W*b* is associated with the line section T*b* to which the line store C*b* belongs, the positive bias voltage +U likewise being applied to its secondary winding II. The *a.c.* voltages and currents to be transmitted are supplied to its primary winding I.

Making reference to the diagrams illustrated in Figure 8, the mode of operation of the circuit illustrated in Figure 5 will now be explained in greater detail. The intermediate stores here take the form of capacitors. The energy transfer processes in this case take place in the form of half cycle oscillations since the transmission paths, as already described also contain series coils. The operation of the switches allotted to the line stores and to the intermediate stores, is illustrated in the diagrams T, K1 and K2. These diagrams correspond to the similarly designated ones in Figure 7. Thus, the switches are operated in precisely the same manner as in the previous circuit discussed.

Due to the effect of the bias voltage +U applied to the secondary windings II of the transformers W*a* and W*b*, exclusively positive voltages can be developed across the capacitors C*a* and C*b* operating as line stores, *i.e.* their charges can only be of positive polarity. Consequently, during the initial simultaneous operation of the switches 1*k*1 and 2*k*2 when charging up the capacitors C1 and C2 serving as intermediate stores, the charging current always flows through the rectifiers 1G1 and 2G2 in the forward direction. During the subsequent simultaneous operation of the switches 2*k*1 and 1*k*2, the capacitors C1 and C2 are discharged. In this case, the discharge currents pass through the rectifiers 2G1 and 1G2 in the forward direction too.

As already indicated, where rectifiers are present in the transmission paths in the manner described, it can be arranged that energy transfer from and to the stores, which process commences with the switching through of the transmission path concerned, is already completed before the transmission path is broken by the opening of one of the switches *via* which it is made. Where capacitors are used as line stores and intermediate stores, and where inductive coils are included in the transmission path, to achieve the above effect the particular transmission path must form an oscillatory circuit so tuned that the period of a half wave at its resonant frequency is shorter than the shortest interval for which the transmission path itself is switched through. It must be pointed out that a wide tolerance can be permitted on the tuning of the oscillatory circuits concerned. Conveniently, the period for which a transmission path is switched through will be determined by the time of operation of the switch, allotted to an intermediate store, *via* which the transmission path leads.

An example of the behaviour of the voltages occurring across the capacitors C*a* and C*b* in this instance and of the currents associated with the capacitors C1 and C2, is given in the diagrams *u*C*a*, *u*C*b*, iC1 and

iC2 of the Figure 8, already mentioned. These diagrams correspond to the similarly designated diagrams of Figure 7. A comparison shows that as distinct from these latter diagrams, here the voltages and current changes have in each case been completed within half the time of operation of the appropriate switch (allotted to an intermediate store) 1*k*1, 1*k*2, 2*k*1, 2*k*2. These voltage and current changes in each case signify discharge of one of the capacitors involved in the transfer process and the charging up of the other.

Loss of charge back to the delivering capacitor is prevented by the presence of rectifiers in the transmission paths. Consequently, wide tolerances are permissible on the operating times of the centrally located switches. Changes in the tuning of the oscillatory circuits due to capacitance changes associated with parametric amplification, such amplification being effected for instance with the aid of a capacitor store serving as intermediate store, have no direct influence on the necessary operating times for the switches concerned. The intermediate stores, like the capacitors serving as parametric amplifiers, advantageously receive voltages of exclusively one polarity. The switches *k*1 and *k*2 also illustrated in the circuit of Figure 5, serve to short-circuit the capacitors C1 and C2 serving as intermediate stores. Conveniently, they are both operated simultaneously, prior to the commencement of energy transfer between two line stores. The time for which they are operated can be shorter than the time of operation of the other centrally located switches.

Figure 9 illustrates how a capacitor consisting of several sub-capacitors and operating as a parametric amplifier, can conveniently be constructed. The capacitor illustrated there consists of four sub-capacitors C11, C12, C13 and C14 arranged in the form of a bridge circuit. One pair of opposite junctions between the sub-capacitors serves to provide the connections for the capacitor proper. Across the two other opposite connections marked E, a pump voltage is applied in order to produce a change in the capacitance of the sub-capacitors. Varactors are one example of a type of capacitor which can be voltage-controlled in this fashion, they are in fact semiconductor diodes which are operated in the blocking region. The control voltage applied across the terminals B is divided amongst the intervening arms of the bridge by appropriately dimensioning the sub-capacitors, in a manner such that no voltage difference is produced between the other two opposite connections. Consequently, the external circuit in which this variable capacitor is connected remains uninfluenced by the pump frequency.

Figure 10 illustrates how a coil acting as a parametric amplifier can conveniently be constructed. In the case considered, the coil has two sets of two windings which are magnetically coupled with one another. These windings are designated W1, W2, W3, and W4. *Via* the terminals F, a pump voltage may be applied to the windings W3 and W4. This pump voltage produces currents at pump frequency which pass through the two windings considered in opposite directions. The voltages induced in the two windings W1 and W2 by the pump voltage, cancel each other out. Thus the pump frequency does not appear across the connection *m*. Thus, the windings W1 and W2 situated between these two connections *m* may be inserted in the energy transmission path as desired without causing the appearance of the pump frequency in the transmission path.

In a circuit in accordance with the invention, any two line sections pulse-linked *via* intermediate stores operate in duplex fashion. If parametric amplification is effected on the lines described, then the two line sections concerned constitute a duplex amplifier.

It is pointed out that because of the excellent degree of control afforded by a parametric amplifier, the gain can be made dependent in each case upon the attenuation of the particular line sections to be linked. If rectifiers are inserted in the transmission paths, then the changes in resonant frequency occurring with change in gain in any given oscillatory circuit, can be ignored. The facility of changing the gain is of particular interest where the line sections lead to subscriber stations, because with subscriber lines the attenuation frequently varies from one line to the next. By this means, it is possible to adjust the loudness of conversations conducted *via* each particular connection to a common value for all subscribers. An indication of the fact that the line sections considered are subscriber lines, is given in Figures 1 and 5 by the schematically illustrated subscribers stations.

Hitherto, connections extending *via* the same two multiplex rails have been considered. In exchange systems which have larger numbers of subscribers, frequently several pairs of multiplex rails are provided and these can be connected with one another *via* coupling networks equipped with switches. A particular group of subscribers can be connected to each pair of multiplex rails, (*e.g.* see British Patent No. 814,183 Figure 3 of the Provisional Specification). Even where such coupling networks are provided, it may be convenient to effect

energy transfer between subscribers connected to different pairs of multiplex rails, in a manner in accordance with the present invention. Conveniently, two of the central intermediate stores belonging to the two pairs of multiplex rails will be employed. The particularly wide tolerances of switch operating times and on the tuning of the oscillatory circuits developed, permissible with certain of the circuit designs in accordance with the invention, are a particular advantage in the application since it is more difficult than in the simple case to maintain high tolerances where several pairs of multiplex rails are concerned.

In the foregoing description of circuits in accordance with the invention, the construction of the switches used and of the control units which control the switches, was not discussed in detail. This is because such switches and control units are already known (see French Patent No. 1,072,144 and U.S. Patent No. 2,936,337).

As already indicated, a circuit in accordance with the invention has the advantage that emergency operation through a single multiplex rail is possible. Further information will now be given as to how such emergency operation is effected.

For linking line sections connectable to the same two multiplex rails, in this case only those energy transfer processes are carried out, the transmission paths for which extend through a single one of these rails. Consequently, only those of the switches *via* which the line sections are connectable to the single multiplex rail now in use, need be supplied with control pulses. This yields the further advantage that certain faults which may arise in the units producing the redundant control pulses are rendered ineffective. The control pulses for the switches allotted to the line sections are frequently produced using a rotary memory supplying the addresses of line sections handling outgoing traffic and using a similar rotary memory supplying the addresses of line sections handling incoming traffic (see for example Patent Specification No. 981,335). Two such rotary memories are indicated in the circuit of Figure 1. They are designated *Uab* and *Uan* respectively. If only one multiplex rail is in operation, then the control pulses for controlling the switches allotted to the line sections need come only from that rotary memory in which, otherwise, exclusely the addresses of line sections handling traffic in that direction (outgoing/incoming) which corresponds to the particular multiplex rail now in sole use (outgoing multiplex rail/incoming multiplex rail) circulate. Thus, if for example only the outgoing multiplex rail *Mab* is in use, only the rotary memory *Uab* is required, this normally only containing the addresses of line sections handling outgoing traffic. However, in this special instance it must accommodate the addresses of all the line sections which happen to be involved in the connections existing at a given instant. If at this time the other rotary memory suffers some fault, the connections remain uninfluenced. Conversely, this means that in the event of a fault in one of the two rotary memories normally used, emergency operation is always possible through the operative rotary memory and the corresponding multiplex rail. For instance, if the rotary memory *Uan* is faulty, all energy transfer processes will take place *via* the outgoing multiplex rail *Mab*. The switches allotted to the line sections involved must then receive their control pulses from the unaffected rotary memory *Uab*. It should be added too, that defects or faults in other devices can similarly be nullified by employing only one multiplex rail. In order to establish connections between line sections *via* a single multiplex rail only, the necessary energy transfer processes can be put into effect in the following manner. The transfer processes involve both the intermediate stores which are connectable to this multiplex rail. For energy transfer, in each case first of all only the first of the two line stores involved is connected to the multiplex rail, this then giving way to the connection of the second store only and, finally to the connection of exclusively the first store again. Thus, in the circuit of Figure 1 first of all only the line store *Ca* is connected to the multiplex rail *Mab*, then only the line store *Cb* and after that only the line store *Ca*. During the time of connection of the first line store, energy transfer takes place from it to the first intermediate store S1 which is also temporarily connected to the multiplex rail at this time. During the connection of the second line store *Cb*, energy transfer takes place from it to the second intermediate store S2 when it is likewise temporarily connected, whereupon, in staggered sequence, the intermediate store S1 is again temporarily connected and energy transfer takes place from it to the line store *Cb*. When the first line store *Ca* is again connected to the multiplex rail, energy transfer to it from the second intermediate store S2, likewise temporarily connected to the rail, takes place. At this point, the two line stores *Ca*, and *Cb* have exchanged their energy contents. The two intermediate stores S1 and S2 involved are now ready for energy exchange between other line stores. In this way, the necessary energy transfer processes associated with several connections can be carried out through one multiplex rail and the intermediate stores

until, depending upon the scanning frequency governing the connections, energy transfer processes have to be repeated for the first connection considered. This is followed by another energy transfer process for the second connection and so on.

Intermediate stores of different types can be used for these energy transfer processes too, in the manner already described. The other embodiments, described earlier, can also be used where energy transfer through a single multiplex rail is involved.

The sequence of the energy transfer processes in each case associated with a connection and conducted through a single multiplex rail, is indicated in detail in Figure 11, where an illustration is also given of how the stores allotted to the line sections to be interconnected and to their associated line stores are operated; an illustration is also given of how the switches allotted to the intermediate stores should be operated. The operation of the switches *abta* and *abtb* allotted to the line sections *Ta* and *Tb* is indicated in the diagram marked T. The switch *abtb* is operated twice and the switch *abta* once only. First to be operated is the switch *abtb*. In principle, the switch *abta* could be operated first, but then it would be operated twice. During the time of operation of the switch *abtb*, the switch 1*k*2 belonging to the intermediate store S2 is also temporarily operated during the period of operation of the switch *abtb*, as the diagram K2 shows. During the period of operation of the swich *abta*, the switches 1*k*1 and 1*k*2 belonging to the intermediate stores S1 and S2 are alternately operated. This is shown in the diagrams K1 and K2. Then, the switch *abtb* is operated a second time and during the course of this the switch 1*k*1 is also operated. The times of operation of the switches 1*k*1 and 1*k*2 allotted to the intermediate stores are here again no more than half the times of operation of the switches *abta* and *abtb* allotted to the line sections. If capacitors are employed as intermediate stores and an inductive coil is included in the particular transmission path, the energy transfer in this case takes place in the form of a half-cycle oscillation.

The short-circuiting of capacitors serving as intermediate stores, something which has already been mentioned, will in this case conveniently be effected during the period in which the first capacitor e.g. *Cb* is connected. Once again, switches *k*1 and *k*2 are provided for this purpose. Their operating times are indicated in the diagrams marked K1 and K2. These operating times fit in well with the other operating times if they are no more than half the operating times of the switches allotted to the line stores. They may in fact be even shorter since no matching to the time of a half-cycle oscillation is required in this case. Accordingly, the operating time of the switch *abtb* can be reduced.

Making reference to the diagrams *u*C*a*, *u*C*b*, *i*C1 and *i*C2, the behaviour of the voltages across the capacitors serving as line stores and the behaviour of the currents associated with the capacitors serving as intermediate stores, is illustrated. These capacitors are C*a*, C*b*, C1 and C2 in that order. The diagram *u*C*b* illustrates the behaviour of the voltage across the capacitor C*b*. It will be seen that here too the voltage initially present disappears when the switch 1*k*2 is operated. Simultaneously, as the diagram *i*C2 shows, the capacitor C2 is charged up by a current. During the time of operation of the switch 1*k*1, the capacitor C*a* is discharged in accordance with diagram *u*C*a*, the capacitor C1 simultaneously being charged up as the diagram *i*C1 shows. During the subsequent period of operation of the switch 1*k*2, the capacitor C2 is discharged as diagram *i*C2 shows. At the same time the capacitor C*a* is charged up, see diagram *u*C*a*. During the second period of operation of the switch 1*k*1, the capacitor C1 is discharged in accordance with diagram *i*C1. At the same time the capacitor C*b* is charged up, see diagram *u*C*b*. The voltages across the capacitors C*a* and C*b* at the commencement of the energy transfer process, were different, the capacitor C*a* having the lower voltage and the capacitor C*b* the higher one. On completion of the energy transfer processes just considered, the capacitor C*a* has the higher voltage across it and the capacitor C*b* the lower one. Thus, here too the voltages and charges associated with the capacitors serving as line stores have been exchanged in the course of energy transfer.

In the foregoing manner, energy transfer processes for a connection made using the circuit illustrated in Figure 1 can be carried out. In this circuit, no rectifiers are included in the transmission paths. Energy transfer processes of this type can also be carried out where rectifiers are involved e.g. in the circuit of Figure 5. Here too only one multiplex rail is in use. For the sake of clarity, a special figure has been provided in which, in the form of an extract from the circuit of Figure 5, only those devices are illustrated which are to be used in the case under consideration. This is Figure 12.

The circuit elements common to Figures 5 and 12 and similarly referenced are *Ta*, *Wa*, *Da*, *Ac*, *Ca*, *Tb*, *Wb*, *Db*, *b*C and *Cb*. Certain other circuit elements are common to Figures 5 and 12 but are differently referenced. Thus, the elements referenced *La*, *Lb*, *abta*, *abtb*, *Mab*, *Lab*, 1G1, 1*k*1, C1,

$k1$, $1k2$, 1G2, C2 and $k2$ in Figure 5 respectively correspond to the elements referenced *Lia*, *Lib*, *ta*, *tb*, *vt*, Lz, G1, $1k1$, *Sa*, *ka*, $2k2$, G2, *Sb* and *kb* in Figure 12, these elements being similarly connected in both figures. The switches $1k2$ and $2k1$ are common to Figures 5 and 12 but are differently connected in these Figures.

Figure 12 shows only those circuit elements which are actually used in emergency operation. Thus the multiplex rail *Man* is omitted since it is not used in emergency operation.

In the circuit illustrated in Figure 12, each intermediate store is connectible to the multiplex rail *via* two switches which are in series with differently polarised rectifiers so that with the aid of these switches the correct rectifier for the desired energy transfer can be placed in the transmission path. The two rectifiers used are designated G1 and G2. The intermediate store *Sa* has the switches $1k1$ and $2k1$ and the intermediate store *Sb* two switches $1k2$ and $2k2$. If for connecting the intermediate stores to the multiplex rails, switches are used which in themselves permit energy transfer in the desired direction only and therefore at the same time embody the rectifier function, separate rectifiers are not required.

Low-pass filters are connected before the capacitors *Ca* and *Cb* serving as line stores, these filters embodying the chokes *Da* and *Db* and the capacitors *aC* and *bC*. To the line section *Ta* having the line store *Ca*, belongs the transformer *Wa*. To the secondary winding II of this transformer the positive bias voltage +U is applied. The a.c. voltages and currents to be transmitted are supplied to its primary winding I. Similarly, the transformer *Wb* belongs to the line section *Tb* having the line store *Cb*, to the secondary winding II of this transformer likewise the positive bias voltage +U being applied. The a.c. voltages and currents to be transmitted are fed to its primary winding I. Due to the effect of the bias voltage applied to the secondary windings II, only positive voltages can develop across the capacitors *Ca* and *Cb* serving as line stores.

Making reference to the diagrams T and K of Figure 13, it will be seen how the switches $1k1$, $2k1$, $1k2$ and $2k2$ belonging to the intermediate stores and the switches *ta* and *tb* belonging to the line sections to be interconnected, should be operated when two intermediate stores are involved in all the connections. During the time of operation of the switch *ta*, first of all the capacitor *Sa* is charged up by the switch $1k1$; the charging current passes through the rectifier G1 in the forward direction. During the time of operation of the switch *tb*, the capacitor *Sb* is charged up *via* the switch $1k2$, the current passing through the rectifier G1 in the forward direction. Immediately, the capacitor *Sa* is discharged through the switch $2k1$ and the rectifier G2, the current flowing through the latter in the forward direction. Finally, *via* the same rectifier G2, (current flow in the forward direction) and the switch $2k2$, the capacitor *Sb* is discharged during the second period of operation of the switch *ta*. For short circuiting of the capacitors *Sa* and *Sb* using the switches *ka* and *kb*, the same time intervals as referred to earlier are available. The switches $1k1$, $2k1$, $1k2$ and $2k2$ are operated in an appropriately modified fashion when two intermediate stores are provided for each connection.

Due to the use of rectifiers in the transmission paths, in the manner proposed in the foregoing, it can also be arranged that energy transfer to the line-stores, commencing with the switching through of the transmission path concerned, is already completed before the transmission path is broken by the opening of one of the switches through which the energy passes. When using capacitors as line stores and as intermediate stores, and when inductive coils are included in the transmission path, the particular transmission path developed should constitute an oscillatory circuit so tuned that the period of a half-wave at its resonant frequency is shorter than the shortest time interval for which the transmission path itself is switched through. Where the timing of the particular oscillatory circuit is concerned, a wide tolerance is permissible. Conveniently, the period for which the transmission path is switched through will in each case be determined by the time of operation of that switch (allotted to an intermediate store) *via* which the transmission path extends.

An example of the behaviour of the voltages and currents appearing in this case at the intermediate stores *Sa* and *Sb*, and of the behaviour of the voltages appearing across the line stores constituted by the capacitors *Ca* and *Cb*, is contained in the diagrams *uCa* . . . *uSb* of Figure 13. A number of appropriately designated diagrams corresponding to these are illustrated in Figure 11. A comparison reveals the distinction that in the case under consideration the voltage and current changes are in each case completed within half the time of operation of the appropriate switch ($1k1$, $1k2$, $2k1$ and $2k2$) allotted to an intermediate store. These voltage and current changes in each case represent the discharge of one of the capacitors involved and the charging up of the other. Any tendency for reverse discharge is suppressed by the rectifiers inserted in the transmis-

sion paths. Wide tolerances are permissible on the operating times of the centrally located contacts. Changes in the tuning of the oscillatory circuits due to capacitance changes taking place with parametric amplification, such amplification being effected for instance with the aid of a capacitor acting as intermediate store, have no direct influence on the necessary operating times of the switches concerned. The intermediate stores such as the capacitors acting as parametric amplifiers, are moreover conveniently supplied with voltages of one polarity only.

It is pointed out that the capacitors employed as intermediate stores in the circuit of Figure 12 can likewise be replaced by intermediate stores of some other type. For instance, that part of the circuit situated below the points A and B can be replaced by the circuit illustrated in Figure 14. The contact operations portrayed in the diagrams T and K of Figure 11 remain unaltered in this case. However, the contacts *ka* and *kb* are omitted.

During the aforedescribed energy transfer processes, due to the use of two intermediate stores which are common to all connections, the addresses of the line sections in each case linked together must be recorded in the rotary memory in direct succession. This limiting condition can be avoided if the energy transfer processes involved in each connecting extending *via* the multiplex rail take place *via* two intermediate stores specially provided for this particular connection. The presence of all these intermediate stores is indicated in Figure 12 by the multiple connection sign *vs*. In such an arrangement, the first and second of the line stores concerned are connected to the multiplex rail alternately. During the time of connection of the first line store, the first two intermediate stores are connected to the multiplex rail alternately, first of all energy transfer taking place from the first line store to the first intermediate store and subsequently the first line store being fed with energy previously stored in the second intermediate store. During the time of connection of the second line store, the second and first intermediate stores are alternately connected to the multiplex rail. In this case, there is first of all energy transfer from the second line store to the second intermediate store and subsequently from the first intermediate store to the second line store. The energy previously transferred to the second intermediate store remains there until the next occasion upon which the first line store is connected to the multiplex rail.

Between successive periods of connection of the two line stores involved in the connection, there may be pauses. This means that the addresses of the line sections in each case involved in a connection need not be recorded in the rotary memory in direct succession. Conveniently, but not necessarily, there will be an interval between these addresses corresponding to half a rotary cycle. For any connection, it is merely necessary to have the two addresses of the line sections concerned in the rotary memory at any positions. During the pauses occurring between the periods of connection of the two line stores involved in one and the same connection, other line stores and other intermediate stores can be connected to the multiplex rail in the course of other connections. If the intermediate stores are in the form of capacitors, then here too it may be necessary to short-circuit these at specific instants. Conveniently, this will be effected during the pauses between the times of connection of the line stores belonging to the particular connection. However, it must be ensured that no charge delivered to a line store in the course of a connection is lost in this way. Consequently, short-circuiting should be effected in each case directly after the discharge of intermediate store into a line store. Appropriate times are indicated in the diagram K of Figure 13, the times of operation of the contacts *kb* and *ka* being indicated. Where the intermediate stores are in the form of cores, the reset pulses to these cores should be supplied at similar instants.

Apart from the pauses mentioned, the sequence of energy transfer processes involved in a connection corresponds to the sequence of similar processes illustrated in Figure 11. A common feature of all these energy transfer processes is that the two centrally located intermediate stores involved in the energy transmission path are alternately connected to the multiplex rail during the period of connection in each case of one of the two line stores concerned to this same multiplex rail, and that the switches are operated in a sequence such that during the simultaneous operation of a switch allotted to a line section and of one of the switches allotted to the intermediate stores, energy transfer only takes place through a previously discharged store.

At this point an explanation will be given of how switching can be carried out so that energy transfer processes normally conducted through both multiplex rails are modified and the associated transmission paths are conducted through one multiplex rail only. Switching in this manner should be carried out for instance when a multiplex rail has become faulty due to short-circuiting either to earth or *via* some other

path. After switching, exclusively the other multiplex rail remains in operation. In the circuit illustrated in Figure 1, the multiplex rails *Mab* and *Man* are linked to the monitoring unit U1 which, in the event of a fault in one of the two multiplex rails, produces a signal to effect switching. The monitoring unit can be constructed using switches having a threshold action for instance, these responding when the applied voltages continuously exceed a specific level. The signal produced by the monitoring unit is passed to the control unit Q associated with the exchange system, which brings about the change in operation. Also provided is the monitoring unit U2 which is linked to lines leading from the control unit Q to the rotary memories *Uab* and *Uan*. *Via* these lines, digits which are to be stored in the memories in the course of exchange processes and which form part of the addresses of line sections, are transmitted, as also are commands for erasing such digits and addresses. If the traffic through these lines increases to an abnormal level or disappears altogether, then this is an indication that a fault has occurred either in a rotary memory or in a multiplex rail. The monitoring unit U2 contains counters which detect any such build-up in the frequency of these processes or detect the absence thereof. In this event, the monitoring unit U2 transmits a signal to the control unit Q in response to which this unit at least temporarily modifies the energy transfer processes so that the transmission paths are conducted through one multiplex rail only, thus using only one rotary memory. If the abnormality in digit storage, or erasting, then disappears, the fault will have been overcome. If the abnormality does not disappear, however, then a switch for operating exclusively with the other multiplex rail and the other rotary memory can be made, when the faults should disappear.

A monitoring unit U2 can also be employed to supervise suitable other processes. Generally speaking, these processes are of the type which take place relatively seldom in comparison to processes such as the operation of switches, being only a random occurrence (see German Patent 1,130,865 and German explanatory document 1,041,079).

Some indication must now be given of how traffic in the exchange system is influenced by the use of one multiplex rail instead of two for the energy transfer processes. For this, we will consider the diagrams T in Figures 6 to 8 and 11. Figures 6 to 8 relate to energy transfer processes conducted through two multiplex rails, whilst Figure 11 relates to the conduction of these processes through one multiplex rail only. As a comparison between the diagrams T in Figures 6 to 8 and the diagram T in Figure 11 shows, all other things being equal, a considerably longer total time is required for operating the switches allotted to the line sections in order to bring about exchange of charge between the capacitors serving as line stores, if only one multiplex rail is used; this is because the switches allotted to the line sections have to be operated in succession. Thus, for one and the same connection the single rotary memory must now record more than one address for these switches. Normally, *i.e.* with two multiplex rails in use, one address will suffice, namely that of the line section handling outgoing traffic or that of the line section handling the incoming traffic. Since in this case any one connection requires more storage space than usual, the total number of connections which can exist at one and the same time is inevitably smaller. Thus, switching to the working of one multiplex rail only results in restriction of traffic.

In given circumstances, this may mean that a number of existing connections have to be broken. Naturally, it is advantageous if one can avoid breaking particularly important connections or connections which for exchange reasons should have special priority. To achieve this end, provision is made for priority connections. The addresses of the line sections associated with priority connections are for this purpose stored at storage positions in the rotary memories, the neighbouring storage positions around which are kept free; the addresses of the line sections connected to the priority line section are transferred to these free positions in the event that one rail operation is necessary. If switching to single rail operation takes place, *e.g.* due to a fault in one multiplex rail, the addresses of priority connections are transferred from the rother rotary memory to the single rotary memory now remaining in operation. The priority connections are thus maintained despite switching to single rail operation. This is indicated in Figure 1. There, the rotary memories are shown as having wires in which addresses circulate at storage positions designated by *i*, *i*1, *j* and *j*1. Addresses of priority connections may circulate in both rotary memories at the storage positions *j*. Where energy transfer is conducted through two multiplex rails, these addresses are contained in both rotary memories. In the event of switchover due to a fault in the multiplex rail *Man* for instance, the address stored at the storage position *j* in the rotary memory *Uan* must be transferred to the free storage position *j*1 in the rotary memory *Uab*. It can also be transferred to the stor-

age position $t1$ where necessary. It is pointed out that where the operating time of the switches $k1$ and $k2$ is reduced, see diagrams K1 and K2 in Figure 11, the transferred addresses in each case occupy less space than the ones already there. It may be convenient to keep storage positions free only for such time as an appropriately low traffic volume makes it unnecessary to use them.

The artifice of giving priority to certain connections is not an obvious step. It can be employed with appropriate switching processes in most time-division multiplex exchange systems having two multiplex rails. It is particularly convenient to treat trunk connections as priority connections. Again, it is recommended that priority be given to other connections extending to outside exchanges. Connections from or to specific subscribers can also be given such priority; this is especially recommended where PBX exchanges are concerned. In PBX exchanges, very often connections to and from particular subscribers are particularly important and should be given priority.

Attention is drawn to co-pending patent applications No. 17761/64 (Serial No. 1,052,826) and 17762/64 (Serial No. 1,052,827) in which we described and claimed arrangements similar to those described above.

WHAT WE CLAIM IS:—

1. A circuit arrangement for the transfer of energy from a first store to a second store, including first and second store switching means capable of connecting the first store to a first multiplex rail and the second store to a second multiplex rail and including two intermediate stores and intermediate store switching means capable of connecting either one intermediate store to the first multiplex rail and the other intermediate store to the second multiplex rail or said one intermediate store to the second multiplex rail and said other intermediate store to the first multiplex rail, the arrangement being such that in operation the first store is connected to said one intermediate store through the first multiplex rail, and the second store is connected to said other intermediate store through the second multiplex rail and any energy stored in the first and second stores is transferred to the intermediate stores, whereafter said one intermediate store is connected to the second store through the second multiplex rail and said other intermediate store is connected to the first store through the first multiplex rail to complete the energy interchange between the first and second stores.

2. A circuit arrangement as claimed in Claim 1, wherein during operation the first store remains connected to the first multiplex rail and the second store remains connected to the second multiplex rail throughout the energy interchange between first and second store.

3. A circuit arrangement as claimed in Claim 1 or Claim 2, wherein both the first and second stores are connectable to both multiplex rails.

4. A circuit arrangement as claimed in any of the preceding Claims, wherein the arrangement is a time-division multiplex telephone exchange system in which the energy interchange is effected at cyclically repeated intervals and wherein the first and second stores terminate communication lines in the exchange.

5. A circuit arrangement as claimed in Claim 4, wherein the first store terminates the line of a calling station and the second store terminates the line of a called station.

6. A circuit arrangement as claimed in Claim 5, wherein low-pass filters with a cut-off frequency of less than half the frequency of the cyclically repeated intervals are connected between the first and second stores and the respective communication lines.

7. A circuit arrangement as claimed in any of the preceding Claims, wherein the intermediate storage of energy is effected in conjunction with amplification of the energy.

8. A circuit arrangement as claimed in any of the preceding Claims, wherein the first and second stores are capacitors.

9. A circuit arrangement as claimed in any of the preceding Claims, wherein the intermediate stores are shunt inductors.

10. A circuit arrangement as claimed in Claim 9 as appended to Claim 8, as appended to Claim 6, wherein energy transfers to the stores concerned in each case takes place in the form of a quarter cycle oscillation in the transmission path between the stores; and wherein energy transfer from a first or second store capacitor to an intermediate store inductor is followed directly by energy transfer from this inductor to the other capacitor store.

11. A circuit arrangement as claimed in Claim 9 or Claim 10, wherein in parallel with each intermediate store inductor, an auxiliary capacitor is connected which prevents any interruption in current flowing through the inductor on changeover from energy transfer to the inductor to energy transfer from the inductor.

12. A circuit arrangement as claimed in Claim 8, wherein series inductors are provided in the transmission paths between stores which due to their inductance cause energy transfer between the stores con-

cerned to take place in the form of a half-cycle of an oscillation.

13. A circuit arrangement as claimed in Claim 12, wherein series inductors are respectively common to a first and second store.

14. A circuit arrangement as claimed in Claim 12, wherein series inductors are respectively connected in series between a multiplex rail and an intermediate store.

15. A circuit arrangement as claimed in Claim 13, wherein at least a part of each series inductor is situated in each multiplex rail.

16. A circuit arrangement as claimed in any of Claims 12 to 15, wherein a series inductor is connected between each first and second store and the appropriate multiplex rail.

17. A circuit arrangement as claimed in any of Claims 9 to 16, wherein at least one of the inductors is an inductive parametric amplifier.

18. A circuit arrangement as claimed in any of Claims 1 to 8 or 12 to 16, wherein the intermediate stores are capacitive stores.

19. A circuit arrangement as claimed in Claim 18, wherein the capacitive intermediate stores are parametric amplifiers.

20. A circuit arrangement as claimed in Claim 18 or Claim 19, wherein short circuiting switching means are provided for short circuiting the capacitive stores for a period when they are not in use.

21. A circuit arrangement as claimed in any of Claims 1 to 8 or 12 to 16, wherein the intermediate stores are ferromagnetic cores of a material exhibiting remanence and have substantially linear magnetic properties within the range used for energy transfer.

22. A circuit arrangement as claimed in Claim 21, wherein energy transfer from a core serving an intermediate store to a line store is effected with the aid of a read pulse which resets the particular core to a magnetic state corresponding to no energy stored.

23. A circuit arrangement as claimed in Claim 21 or Claim 22, wherein reset pulses are applied to the cores serving as intermediate stores, just before energy is stored in them, which reset pulses reset the cores precisely to the magnetic state corresponding to no energy stored.

24. A circuit arrangement as claimed in any of Claims 1 to 8 or 12 to 16, wherein the intermediate stores are superconductive coils in which a current is induced through coupling coils during the in-storage of energy.

25. A circuit arrangement as claimed in Claim 24, wherein energy transfer from a superconductive coil acting as intermediate store to a first or second store is effected by means of a read pulse fed through a read winding encircling the superconducting coil, which read pulse produces a magnetic field which inhibits superconductivity in the superconductive coil.

26. A circuit arrangement as claimed in any of the preceding Claims, wherein the intermediate store switching means is constituted by four individual switches each capable of connecting one store to a multiplex rail and wherein the time of closure of each of these switches is not greater than half the time of connection of a first or second store to a multiplex rail.

27. A circuit arrangement as claimed in any of the preceding Claims, wherein several lines to be interconnected are subdivided into groups, each of which groups is connectable to a pair of multiplex rails allotted to that group, the appropriate multiplex rails for each connection being connected together *via* switches of coupling networks for energy transfer between line sections of different groups.

28. A circuit arrangement as claimed in Claim 27, wherein in each case two centrally located intermediate stores allotted to the appropriate pairs of multiplex rails, are in each case employed for the energy transfer processes.

29. A circuit arrangement as claimed in any of the preceding Claims, wherein the first and second store switch means and the intermediate switch means are also operable in such a way that energy interchange can be effected by connecting both first and second stores exclusively to either the first or second multiplex rail.

30. A circuit arrangement as claimed in Claim 29, wherein control pulses for the switches allotted to the lines can be produced from a rotary memory provided for supplying the addresses of lines handling outgoing traffic, and from a further rotary memory provided for the production of the addresses of lines in each case handling incoming traffic, wherein during operation the control pulses for controlling the switches allotted to the lines are produced by that rotary memory in which there normally circulates only the addresses of lines handling traffic in a direction (outgoing or incoming) corresponding to the particular direction for which the multiplex rail (outgoing multiplex rail or incoming multiplex rail respectively) now exclusively used is intended.

31. A circuit arrangement as claimed in Claim 29 or Claim 30, wherein the two intermediate stores included in the transmission path, are alternately connectable to the operative multiplex rail *via* central switches during the time for which the

first or second store is likewise connected, and wherein switches are operated in a sequence such that during the simultaneous operation of a switch allotted to a first or second store and one of the switches allotted to the intermediate stores, in each case energy transfer exclusively to a previously discharged store takes place.

32. A circuit arrangement as claimed in Claim 31, wherein during operation first of all only the first store is connected to the multiplex rail, to be followed by the connection only of the second store, then, again, only the first store being connected, wherein during the period of connection of the first store, energy transfer takes place to said one immediate store which is also temporarily connected to the multiplex rail at the same time, wherein during the period of connection of the second store energy transfer takes place from it to said other intermediate store when the latter is temporarily connected to the multiplex rail, in alternation with this said one intermediate store also being temporarily connected and energy transfer taking place from it to the second store, and wherein during the subsequent repeated connection of the first store coincidentally with the temporary connection of said other intermediate store, energy flows from it to the first store so that at this stage the first and second stores have exchanged their energy content with one another and the two intermediate stores employed are now free for energy exchange between two other stores.

33. A circuit arrangement as claimed in Claim 31, wherein the energy transfer processes for each connection extending *via* the operative multiplex rail are carried out through two additional intermediate stores provided for this connection, wherein the first and second stores are alternately connected to the operative multiplex rail, wherein during the period of connection of the first store to the rail, the first additional intermediate store and the second additional intermediate store are alternately connected to the operative multiplex rail, firstly energy transfer taking place from the first store to the first additional intermediate store and subsequently energy previously stored in the second additional intermediate store being transferred to the first store, wherein during the period of connection of the second store the second and first additional intermediate stores are alternately connected to the operative multiplex rail, initially energy transfer from the second store to the second additional intermediate store taking place, then energy transfer from the first additional intermediate store to the second store taking place, the energy transferred to the second additional intermediate store remaining there until the next occasion on which the first store is connected to the operative multiplex rail.

34. A circuit arrangement as claimed in Claim 33, wherein in the interval between the connection of the second store to the multiplex rail and the connection of the first store to the multiplex rail, additional first and second stores and other intermediate stores can be connected to the multiplex rail to effect other connections.

35. A circuit arrangement as claimed in any of Claims 29 to 34, wherein each multiplex rail is linked to a monitoring unit which, in the event of a fault in a multiplex rail, produces a switching signal which transfers the operation of the arrangement from two-multiplex-rail operation to one-multiplex-rail operation.

36. A circuit arrangement as claimed in Claim 30 or any one of Claims 31 to 34 as dependent upon Claim 30, wherein each rotary memory is connected to a monitoring unit which transfers the operation of the arrangement from two-multiplex-rail operation to one-multiplex-rail operation when a fault develops in one of the rotary memories.

37. A circuit arrangement as claimed in Claim 36, wherein the monitoring unit monitors the rate of appearance of addresses in the rotary memories and switches to one-multiplex-rail operation if this rate is too slow or too fast.

38. A circuit arrangement as claimed in Claim 30 or any one of Claims 31 to 37 as dependent upon Claim 30, wherein provision is made for priority connections in the event of one-multiplex-rail operation; wherein the addresses of the priority stations are present in the two rotary memories at storage positions in the neighbourhood of which other storage positions are kept free, and wherein on transfer to one multiplex rail operation these free positions are employed to maintain priority connections.

39. A circuit arrangement as claimed in Claim 38, wherein storage positions are kept free only for as long as an appropriately low traffic volume makes it unnecessary to use them.

40. A circuit arrangement for the transfer of energy from one store to another according to any preceding claim and substantially as described with reference to any of the Figures of the accompanying drawings.

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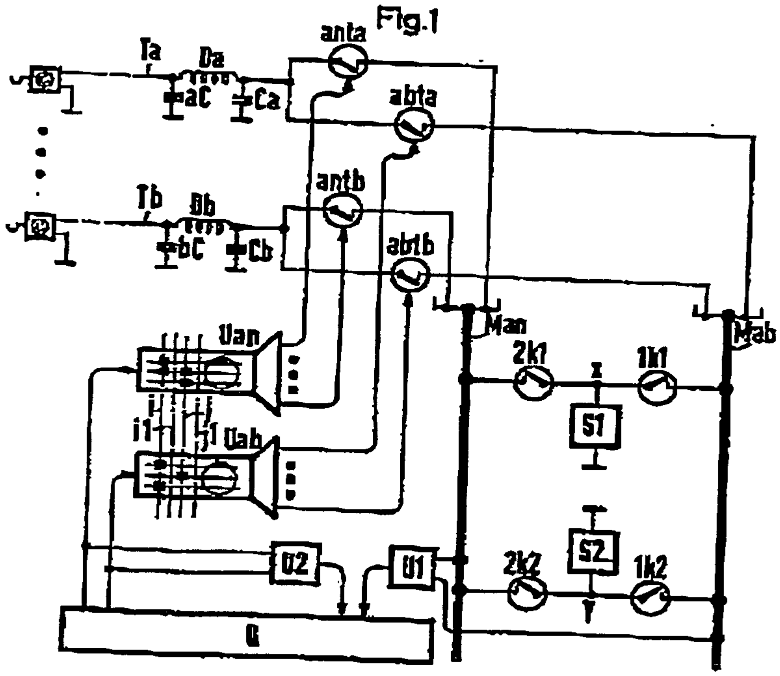
1052828 COMPLETE SPECIFICATION

5 SHEETS *This drawing is a reproduction of the Original on a reduced scale*

Sheet 1



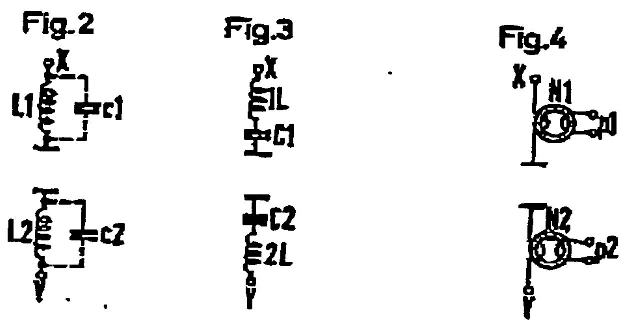


Fig.5.

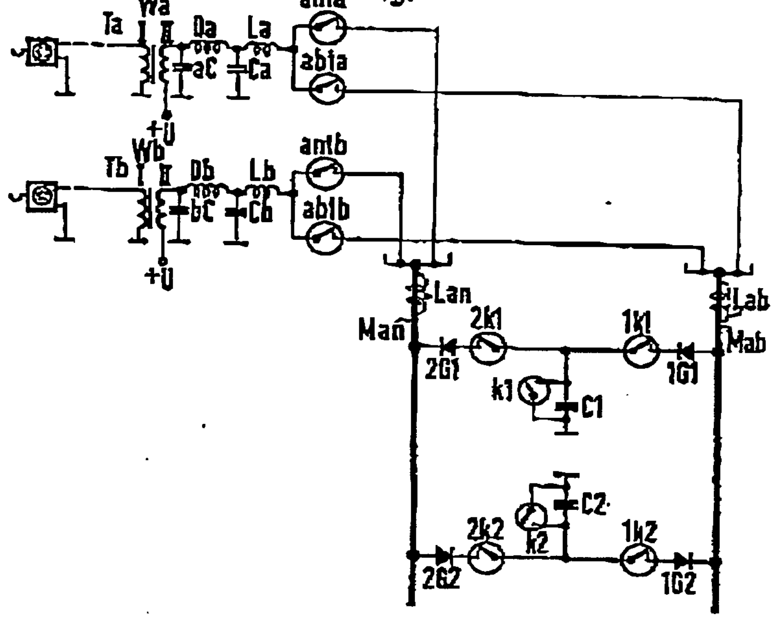


Fig.9

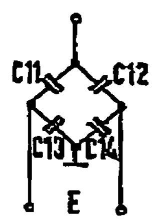
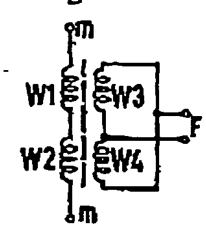
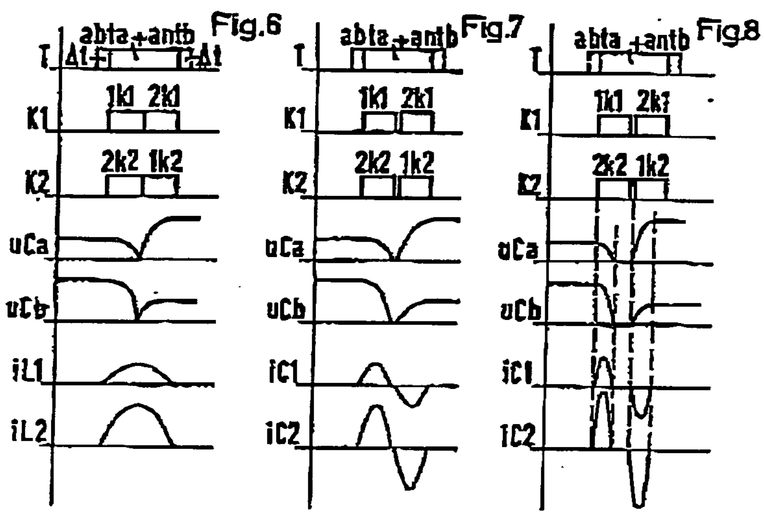


Fig.10



1052828 COMPLETE SPECIFICATION
5 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
Sheets 2 & 3



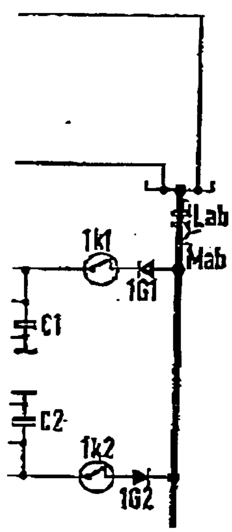
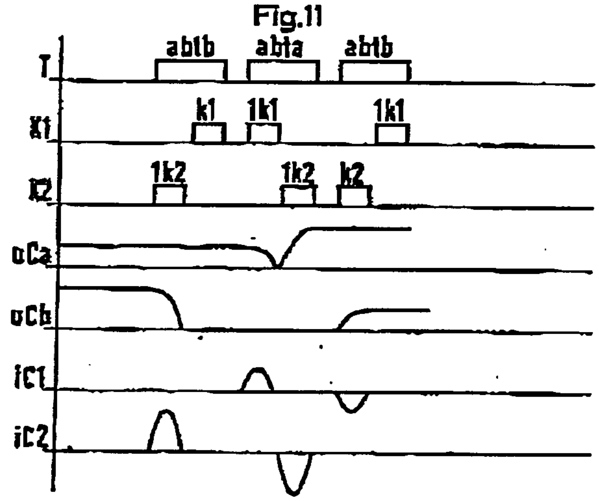
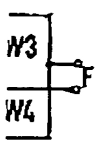
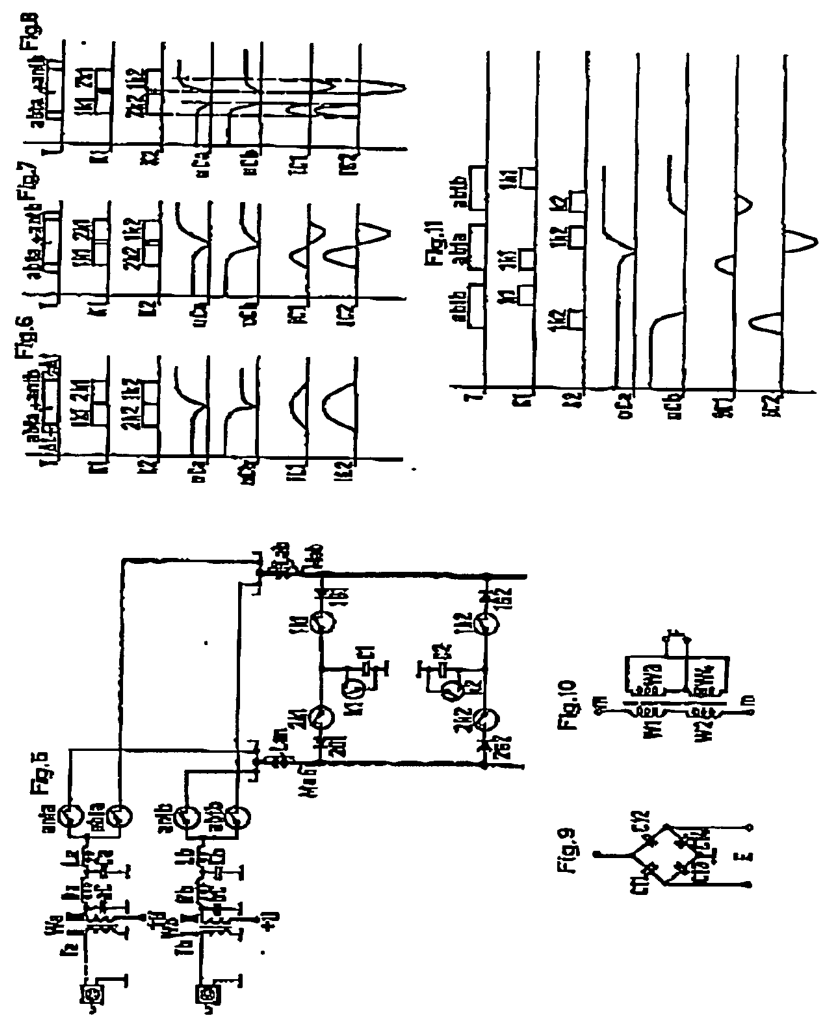


Fig.11





1052826 COMPLETE SPECIFICATION
5 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheets 2 & 3



1052828 COMPLETE SPECIFICATION
5 SHEETS This drawing is a reproduction of the Original on a reduced scale
Sheets 4 & 5

Fig.12

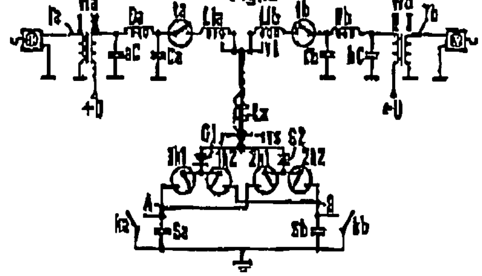


Fig.13

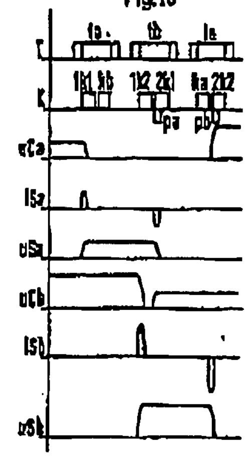
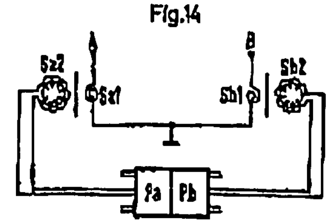


Fig.14



1052828 COMPLETE SPECIFICATION
5 SHEETS *This drawing is a reproduction of the Original on a reduced scale*
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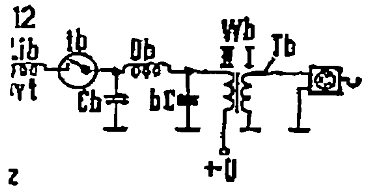
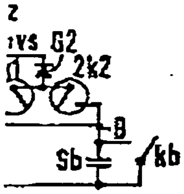


z



.13

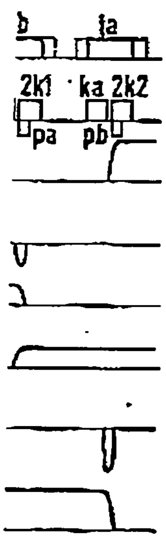


Fig.14

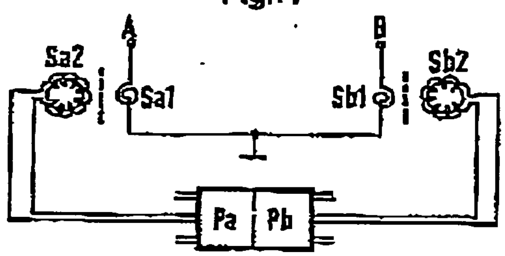
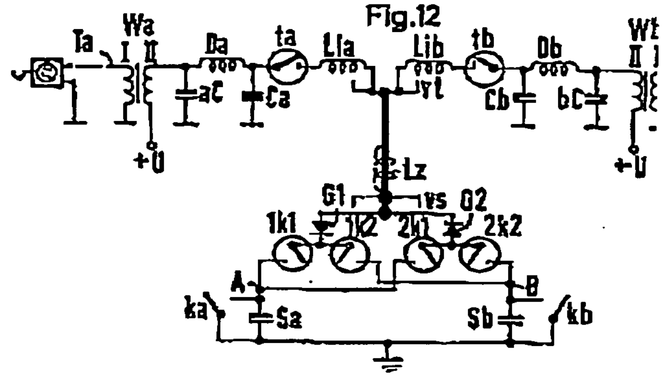


Fig.12


Ta
Wa
I
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1k1
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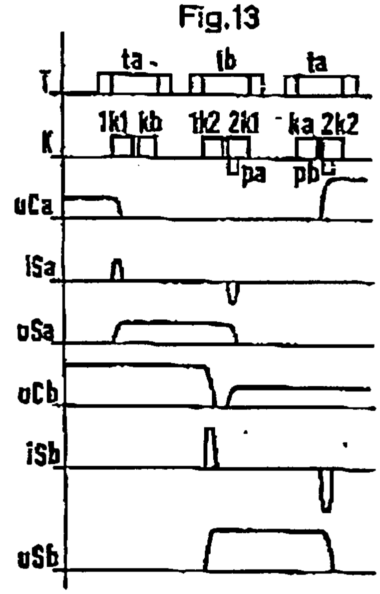
Fig.13


T
ta
tb
ta
K
1k1
kb
1k2
2k1
ka
2k2
pa
pb
uCa
iSa
uSa
uCb
iSb
uSb